A Design Approach for Mass Producible High-Bit-Rate MMIC Transimpedance Amplifiers

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***Abstract*— A full design approach for developing very high-speed transimpedance amplifier (TIA) monolithic microwave integrated circuits (MMIC's) to be economically produced in large quantities is described. As an application example, the letter reports design, experimental performances, yield, and size data for a 5-Gb/s MMIC TIA using a low-cost 0.5-μm GaAs field-effect transistor (FET) technology, showing outstanding experimental performances and optimized for a large-volume industrial production.**

***Index Terms*—Circuit CAD, MMIC's, optical receivers, preamplifiers.**

I. Introduction

OWING to the extraordinary capability of transmitting a great number of data per unit time and to the insensitivity to electromagnetic interferences (EMI), high-bit-rate optical links play an important role in telecommunication development. Moreover, because of a strong demand for high-speed digital services, optical equipment manufactures are now extremely interested in the development of low-cost wideband networks [1]. In such applications, the received light is usually sent to a photodiode, which converts the optical into a current signal. Transimpedance amplifiers (TIA's) transform, with low noise, this current into a voltage signal adequate for a subsequent electronic elaboration. This letter describes a design strategy for developing high-performance and wideband monolithic microwave integrated circuit (MMIC) TIA's to be produced in large quantities. Then, it reports measured performances, yield, and size data of a 5-Gb/s TIA designed with this strategy.

II. MMIC TIA Design Strategy

When designing MMIC's, literature topologies are usually considered, which are then adapted to give the required performances, mainly with cut and try procedures. However, this system is inadequate to develop prototypes of mass producible circuits, since the constraints (minimize size and maximize yield) for a low-cost fabrication are not taken into account. The overall MMIC yield is a product of factors [2], the most important of which are the dc yield $Y_{\rm dc}$ and the parametric [or radio frequency (RF)] yield Y_p. $Y_{\rm dc}$ is particularly sensitive to the total on chip gate width (including field-effect transistor (FET) devices and FET-like diodes) and to the number of via holes [2]. The evaluation of Y_p requires calculations based on process fluctuations and bears statistical and modeling problems described and solved in [2]. From these considerations, the following strategy for developing mass-producible MMIC TIA's was deduced. The design starts again from the analysis of previously reported circuits. This permits the selection of those to be assumed as starting points of the procedure. The second step consists of looking how they can be simplified. This is normally paid in terms of performance degradations and, for determining the parameters to be sacrificed, the designer must have in mind a clear priority scale on the importance of each circuit performance in operating conditions. Then, between the simplified topologies meeting the specifications so revised, he has to choose the simplest one and verify its insensitivity to the process fluctuations. If the result is satisfactory, he can proceed to subsequent steps; if not, he must discover the reasons for sensitivity and try to modify the circuit without compromising its most important performances. When this is not sufficient to achieve the desired results, he must restart from another topology and repeat the procedure until a simplified topology meeting the revised specifications and insensitivity to process fluctuations is obtained. Then, a step still not sufficiently considered in TIA MMIC design is made: the circuit scaling toward higher impedances within the limits imposed by the opportunity of optimizing the achievable amplifier noise. All circuit components are scaled, with exception of those of the output buffers. This operation do not affect gain, bandwidth, and sensitivity to process fluctuations, but permits a reduction of noise, power consumption, and total on-chip gate width.

III. Specific Design of a 5-Gb/s Mass Producible MMIC TIA

Bandwidth, noise, and dynamic range are the most qualifying parameters of optical front-end preamplifiers [3]. So, we decided to develop a 5-Gb/s circuit having a minimum equivalent input noise current, but able to guarantee a dynamic range not smaller than that of the best TIA's for 2.5 Gb/s (described in the literature or commercially available) using the same technology. From a careful market and literature analysis, we concluded that the TI gain was not very important, provided that a minimum level of 57 dBΩ be guaranteed. Single device inverters were discarded for their high noise. So, we adopted a cascode topology which makes available better noise performances without amplifier bandwidth loss. Cascode-type TIA MMIC's were extensively reported in the literature [4], [5] and particularly studied in the frame of the

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TABLE I
DC VOLTAGE (V) AT THE CIRCUIT NODES CALCULATED BY USING TRIQUINT DATA SETS ON PROCESS FLUCTUATIONS FOR $V_{DD} = 6$ V AND $V_{SS} = -5.2$ V

Process Type	Nodes of the Circuit						Process Type	Nodes of the Circuit					
	1	2	3	4	5	6		1	2	3	4	5	6
NMNMNM	-0,62	1,40	3,48	0,76	3,70	3,85	LHHIHI	-0,45	1,35	3,76	0,79	3,87	3,91
HHHIHI	-0,83	1,63	3,04	0,84	3,40	3,65	LHHILO	-0,46	1,33	3,74	0,76	3,84	3,89
HHHILO	-0,84	1,60	3,01	0,79	3,38	3,63	LHLOHI	-0,44	1,30	3,77	0,73	3,88	3,92
HHLOHI	-0,83	1,58	3,05	0,78	3,41	3,65	LHLOLO	-0,46	1,28	3,75	0,70	3,85	3,96
HHLOLO	-0,84	1,55	3,02	0,74	3,39	3,64	LLHIHI	-0,43	1,29	3,79	0,79	3,92	4,00
HLHIHI	-0,79	1,62	3,12	0,85	3,46	3,72	LLHILO	-0,44	1,28	3,77	0,76	3,90	3,98
HLHILO	-0,80	1,58	3,10	0,80	3,45	3,72	LLLOHI	-0,43	1,24	3,80	0,73	3,93	4,01
HLLOHI	-0,79	1,56	3,13	0,79	3,47	3,73	LLLOLO	-0,44	1,22	3,78	0,70	3,91	3,99
HLLOLO	-0,80	1,53	3,11	0,74	3,45	3,72							

ESPRIT 5018 COSMIC program by a large European team, which developed some interesting prototypes for 2.5-Gb/s [6]–[8]. So, we chose as a reference and design starting point the circuit selected by this team [6]. If examined for a large-volume production, almost all of the cascode-type MMIC's available in the literature show yield and size limitations. In fact, they have a relatively low dc yield because of the high number of their elements (e.g., 11 FET's + 8 FET-like diodes + 4 essential via holes in [6]) and of the great total on chip gate width (e.g., 2.8 mm in [6]). Moreover, they have a relatively low RF yield because the dc voltage on the cascode output is very sensitive to process fluctuations. If the cascode drives other amplifying stages, as in [4]–[8], these voltage variations often determine an incorrect RF working of the following stages, by damaging amplifier gain, bandwidth, or dynamic range. This was proven through a systematic yield analysis we performed by using the TriQuint foundry data set on process fluctuations. The analysis also showed that the RF failures were generated by some FET forced by the process fluctuations to work in an incorrect dc condition (e.g., too low V_{ds} or positive V_{gs}).

For reaching very high dc and parametric yields, we simplified the circuit in [6] by reducing the diode number and withdrawing the second gain stage. So, we developed a 1.15 $\times$ 1.15 $\times$ 0.2 mm^3 chip having eight transistors and one diode only, where the cascode is directly connected to the amplifier output buffer which can easily follow the voltage variations without RF performance degradation. The total on-chip gate width was reduced to less than 1.4 mm and only three via holes were used. With data from [2] (a 97% dc yield was assumed for via holes on 200-μm-thick chips), the predicted Y_{dc} was 79.9%, (to be compared with $\sim$66% of [6]). Fig. 1 shows the circuit schematics and Table I gives the dc voltage at each circuit node assuming the TriQuint data set for process fluctuations. Here, NMNMNM shows the nominal circuit condition. No incorrect single device biasing is observed in any case.

The circuit makes use of a double inductor peaking, allowing a drastic widening of the transimpedance bandwidth to be obtained. L_1 produces an increase with the frequency of the amplifier gain by resonating the input transistor capacitance,

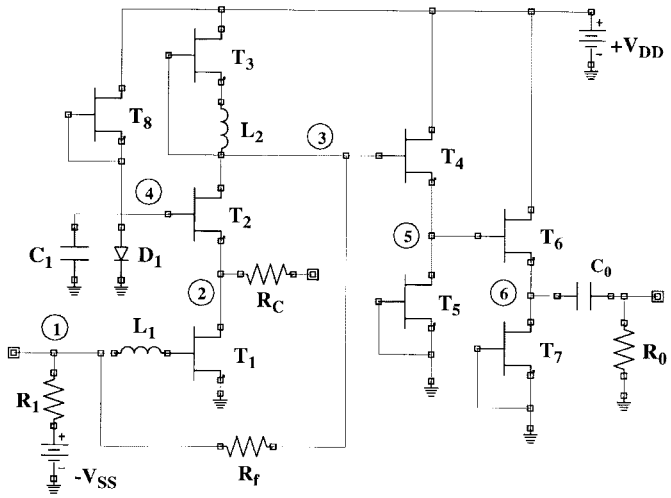

Fig. 1. TIA MMIC electrical circuit.

therefore compensating for the feedback current reduction due to the shunting action of the detector diode parasitic capacitance. L_2 increases the cascode high-frequency load and reduces the current noise in the amplifying devices. The extraordinary bandwidth broadening due to the inductor couple permits the use of very high feedback resistances, allowing a strong reduction of the equivalent input noise current. For this reason our circuit, which uses the F20 GEC-Marconi process [4]–[8], while having a transimpedance bandwidth about twice of that of these MMIC's, still shows a better equivalent input noise current. This explains why when using the circuit (designed and optimized for 5 Gb/s) in 2.5-Gb/s optical receivers an improvement of -2.1 dB in measured sensitivity is obtained, with respect to the result in [6] (-22.4 dBm). Typical on-chip FET dc parameters ($V_{ds} = 3$ V) are: $I_{dss} = 150$ mA/mm, $g_m(I_{dss}) = 140$ mS/mm, $V_p = -1.8$ V (foundry wafer acceptance range on V_p is from -1 to -2.3 V). Typical RF parameters ($V_{ds} = 5$ V, $I_{ds} = 0.5I_{dss}$) are: $g_m = 117$ mS/mm, $C_{gs} = 1.17$ pF/mm, $R_{ds} = 81\ \Omega \times$ mm. Single FET gate widths are ranging between 60 and 350 μm. Noise reduction and greater simplicity of our topology also permit a reduction of the ratio between the amplitude of the minimum detectable signal and the

maximum linear signal amplitude, so resulting in a dynamic range improvement, as explained in [3]. Such an improvement, obtained in spite of the R_f increase [3], proves the better basic linearity of our circuit. A further noise reduction and sensitivity enhancement (~ -2.5 dB) is expected when optimizing the circuit for 2.5 Gb/s (receiver bandwidth $\sim$1.7 GHz). Even if single and multiple inductor peaking are well known in the literature [9], to our knowledge a double inductor peaking of this kind was never used previously in cascode-type MMIC TIA's (laboratory prototypes or, more importantly, circuits for industrial production). The main reason for this is that gain and peaking amplitudes are still too dependent on the process. We solved this problem by using the gain and peaking control resistor R_c. R_c is sufficiently high to prevent any substantial gain or noise degradation for a given dc current amount flowing in the input transistor. If gain and peaking are too low, the resistor free end is connected to $V_{\rm DD}$; if they are too high is connected to the ground or to $-V_{\rm SS}$. In this way, by injecting or subtracting dc current in the input FET, a strong Y_p increase was obtained, in full accordance with PSPICE RF simulations based on the above process fluctuation data set. An external resistor can be added to R_c for making more fine the control. An attractive solution is a laser trimming of R_c based on run sheet data of each wafer. By using our MMIC and a 0.5-pF p-i-n diode (Lasertron Inc.), an optical front-end was constructed. The solid curve **a** in Fig. 2, shows its experimental transfer function. The dashed curve shows the same function as theoretically predicted by a bias-dependent scalable FET linear model we developed for low $V_{\rm ds}$. Curves showing the transfer function for $L_1 = 0$ and for $L_1 = L_2 = 0$ are also given. Curve **b** gives the measured equivalent input noise current density. Experimental receiver parameters are: TI gain = 59 dBΩ, TI bandwidth = 3.5 GHz, electrical dynamic range = 51.2 dB, power consumption = 350 mW. By substituting to our chip a LG1624A (AT&T) a 1.7-GHz bandwidth reduction and a $-$0.5-dB sensitivity enhancement were measured. By using an ATA30011 (the Anadigics Inc. product showing at our knowledge the widest bandwidth) the following receiver parameters were measured: TI gain = 58 dBΩ, TI bandwidth = 2.4 GHz, equivalent input noise current density at 1.4 GHz = 12 pA/Hz$^{1/2}$, electrical dynamic range = 39.6 dB, power consumption = 800 mW. Our MMIC Y_p was tested on 50 chips, having passed the visual inspection, randomly selected on two wafers. Acceptance ranges were: TI gain 59 dB$\Omega\pm$ 0.8 dB, TI bandwidth $>$3.3 GHz, and peaking $<$1 dB. With R_c floating Y_p was 78%. By properly connecting R_c Y_p was 94%. With a simple gain window of $\pm$0.8 dB, Y_p's [5] of MMIC's having an European team topology [8], were between 60% and 68%.

When using more expensive and advanced technologies, such as submicrometric HEMT's or high-cutoff-frequency HBT's, to produce higher speed circuits our topology can greatly enhance bandwidth, dynamic range, noise, gain, and producibility of the state-of-the-art MMIC TIA's.

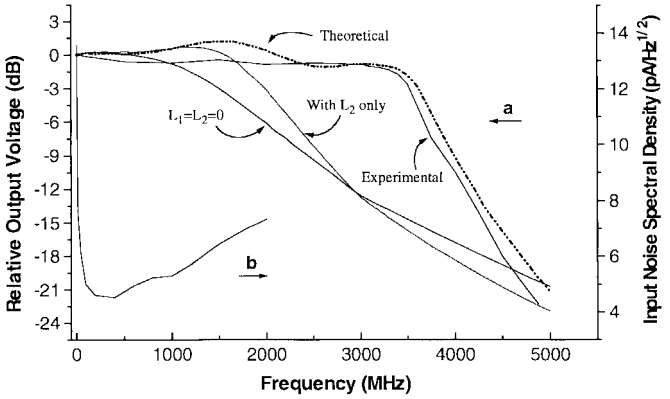

Fig. 2. Solid curve a: experimental transfer function of an optical receiver using our MMIC and 0.5-pF p-i-n diode. Dashed curve: transfer function predicted in the circuit design. Transfer functions for $L_1 = L_2 = 0$ and $L_1 = 0$ are also given. Curve b: equivalent input noise current density.

IV. Conclusion

Starting from general considerations on MMIC producibility, we described a full strategy for developing mass-producible TIA's with improved bandwidth, noise, and dynamic range. Then we reported experimental performances, yield and size data of a 5-Gb/s TIA designed with this strategy and very suitable for developing higher speed circuits.

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